

Image processing is necessary for automated applications employed in fields such as robotics or road traffic surveillance. The main input information is usually visual perception from a camera and this way a system can see. Captured images are then processed and usually used for object detection. The detection process itself is often very complex and computationally demanding. During last several years, many new embedded platforms appeared on the market. They are powerful enough to be able to process images using desired algorithms in real time. As well, they can offer low price and very low power consumption. However, most of image processing related problems have to be speeded-up using various co-processors or custom accelerators. One of the suitable options of building a custom accelerator is an implementation of specialized units in the FPGA part of the hybrid architecture Xilinx Zynq.

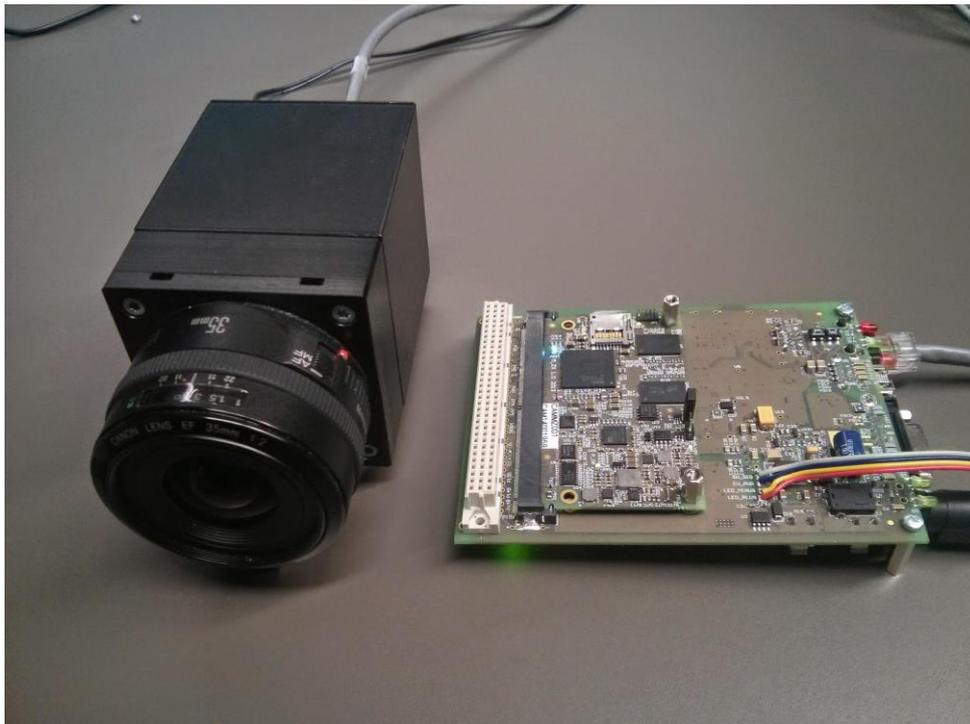


Figure 1: Gigabit Ethernet camera connected to Xilinx Zynq based processing platform

As has been stated, the Xilinx Zynq is hybrid architecture which means it consists of the ARM-based Cortex-A9 dual core CPU which is interconnected via high-speed bus with the Artix-7 FPGA. CAMEA has designed and produced own Zynq-based CPU board attached to as well custom designed carrier board equipped with power source and connectors (see the right part of Figure 1).

As a source of video information we used a camera designed and manufactured by CAMEA (see the left part of Figure 1). The CCD sensor (resolution 752x480) of the camera is controlled by an extra FPGA chip. The framerate is 50 non-interlaced images per second. The data output (and as well control input) interface is gigabit Ethernet. Additionally, the camera has a capability of capturing sequences of images with variable exposure time. Such camera is commonly used in various commercial applications.

Implementation

The camera is connected through Ethernet with the processing platform (see Figure 1). With predefined framerate, the camera is continuously sending captured images over UDP. The ARM-based processor is receiving individual packets and collected parts of image are transferred (over the high speed bus) to the accelerator implemented in the FPGA part. The image is effectively processed there and the detection results are finally transferred back to the CPU part. Additional post-processing of images and subsequent streaming of the detection results (alternatively including input images) is performed here. The final results are transferred over UDP (wired through a router) to a PC where the post-processed images are shown for demonstration purpose.

We successfully implemented face detection algorithm to the FPGA part of the Xilinx Zynq. The face detector is based on the

Waldboost algorithm. A set of weak classifier is evaluated in order to perform detection in every scanning window position in the image. Furthermore, the detector computes up to 12 downscaled versions of an original image and performs detection on them as well in order to find faces of various sizes. The main benefit is that detector works only with a local image buffer for several image lines. It doesn't require additional memory for storing downscaled images – the detector is designed for stream processing. The detector also consumes just a small part of available FPGA resources (less than 1/4 in case of Xilinx Zynq XC7Z010). The very high detection framerate can be later utilized for detecting multiple objects. Moreover, multiple detectors could be implemented into single FPGA.

Testing

The system as whole has been tested in order to prove its capability of real time image processing. The Zynq-based processing system was fed by captured full image data with frame rate 50 FPS. It is able to smoothly detect all faces even in case of many people present in front of the camera (see Figure 2). The system is able to process not just all 50 images per second, but it has reserve to process up to 160 FPS. This indicates Zynq's quality of real-time image processing.

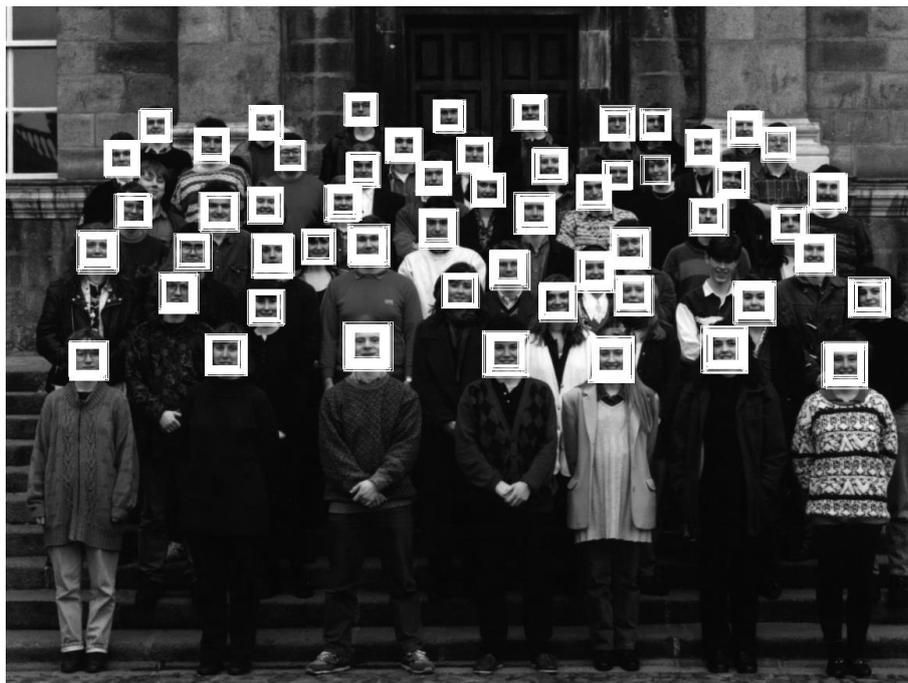


Figure 2: Input image augmented by detection results

Future steps will focus on an implementation of an all-in-one camera system which means the FPGA in the camera will be replaced by a Xilinx Zynq chip. It will then perform both the image sensor control and image processing itself. The basic detection algorithm can be alternatively extended by use of HDR images thank to the multi-exposure camera's capability. The CPU part of the Zynq will then stream processed images or detection results over Ethernet for example to a PC.

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